18. (Amended) The polishing pad used for polishing a semiconductor wafer according to Claim 15, wherein a content of zinc compounds in the porous surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the porous surface layer.

20. (Amended) A polishing pad used for polishing a semiconductor in a mirror polishing process, wherein it is comprises a base layer formed of nonwoven fabric and a porous surface layer, and a content of zinc compounds included in the porous surface layer is 100ppm or less at the ratio of zinc weight relative to the weight of the porous surface layer.

21. (Amended) The polishing pad for polishing a semiconductor wafer according to claim 20, wherein the porous surface layer does not include zinc compounds.

22. (Amended) The polishing pad for a semiconductor wafer according to Claim 14, wherein the porous surface layer is formed of foamed polyurethane.

23. (Amended) The polishing pad for a semiconductor wafer according to Claim 15, wherein the porous surface layer is formed of foamed polyurethane.

24. (Amended) The polishing pad for a semiconductor wafer according to Claim 16, wherein the porous surface layer is formed of foamed polyurethane.

25. (Amended) The polishing pad for a semiconductor wafer according to Claim 20, wherein the porous surface layer is formed of foamed polyurethane.

26. (Amended) The polishing pad for a semiconductor wafer according to Claim 21, wherein the porous surface layer is formed of foamed polyurethane.

27. (Amended) A method for polishing a semiconductor wafer, wherein the polishing is performed by using the polishing pad according to Claim 11.

28. (Amended) A method for polishing a semiconductor wafer, wherein the polishing is performed by using the polishing pad according to Claim 12.

29. (Amended) A method for polishing a semiconductor wafer, wherein the polishing is performed by using the polishing pad according to Claim 13.